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G4A AFGL AMP

(56) Documents Cited
EP 0174231 A1 US 5588118 A US 4395758 A
Computer Shopper, Vol.13, No.1, Jan. 1993, J Bryan, p801(4) Computer Shopper, Vol.12, No.1, Jan. 1992, Winn L. Rosch, p.487

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(54) Abstract Title
Processing arrangements

(57) A processing arrangement for a computer comprising:
first processor means (1) for processing a first set of instructions; and
second processor means (2) for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means (2) is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

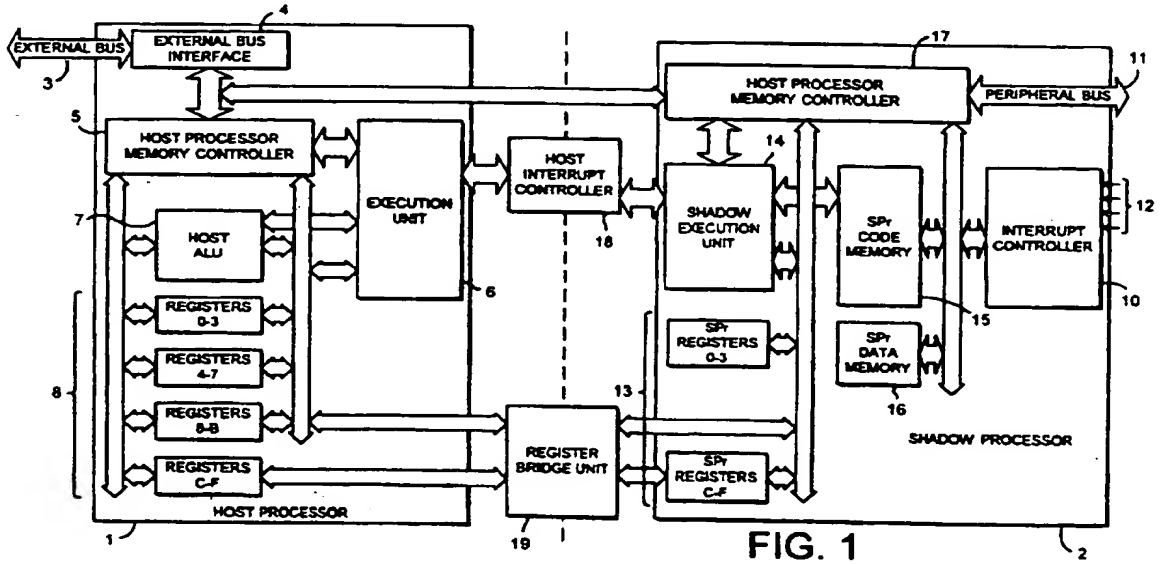

FIG. 1

GB 2 343 269 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

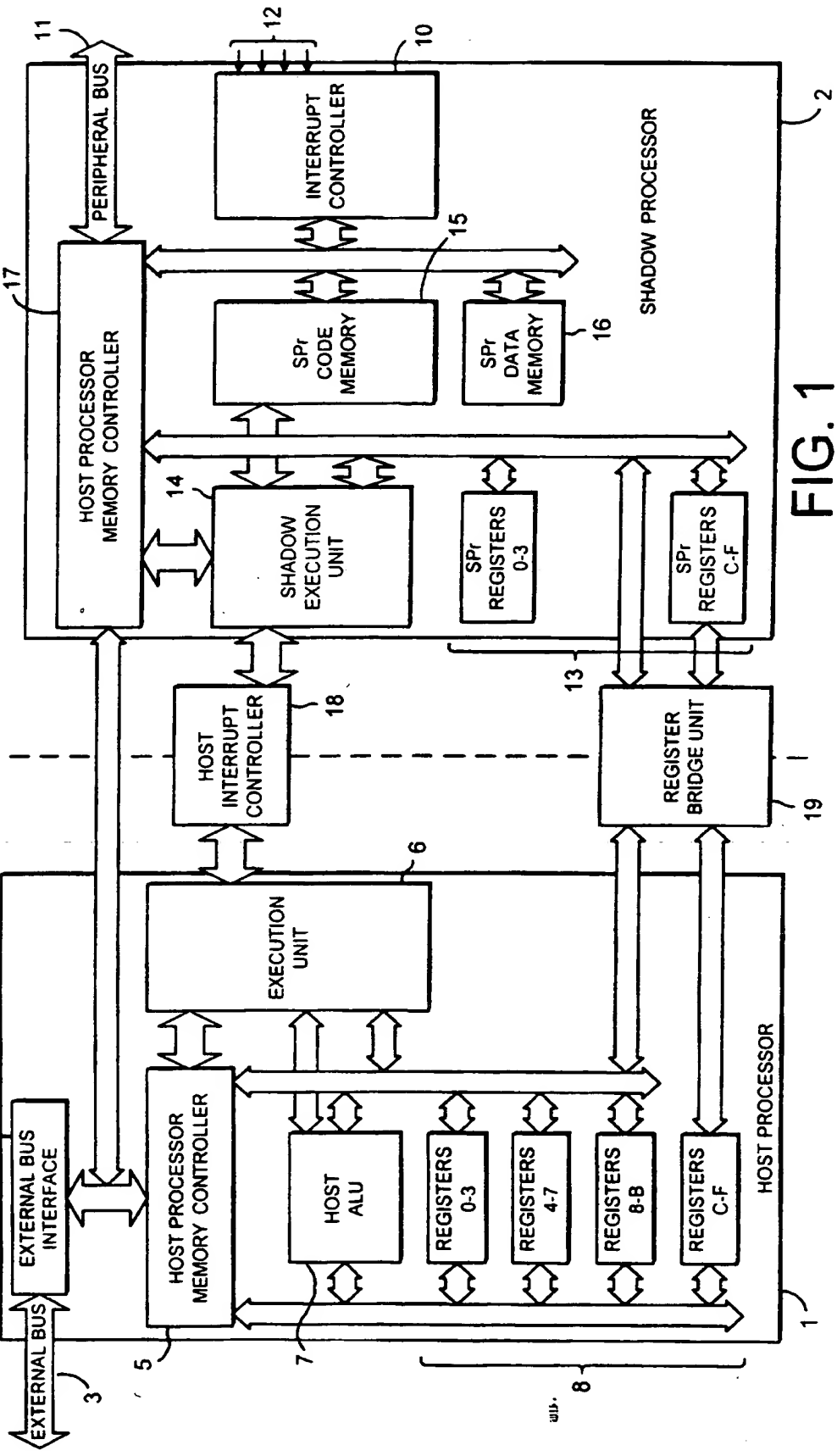

FIG. 1

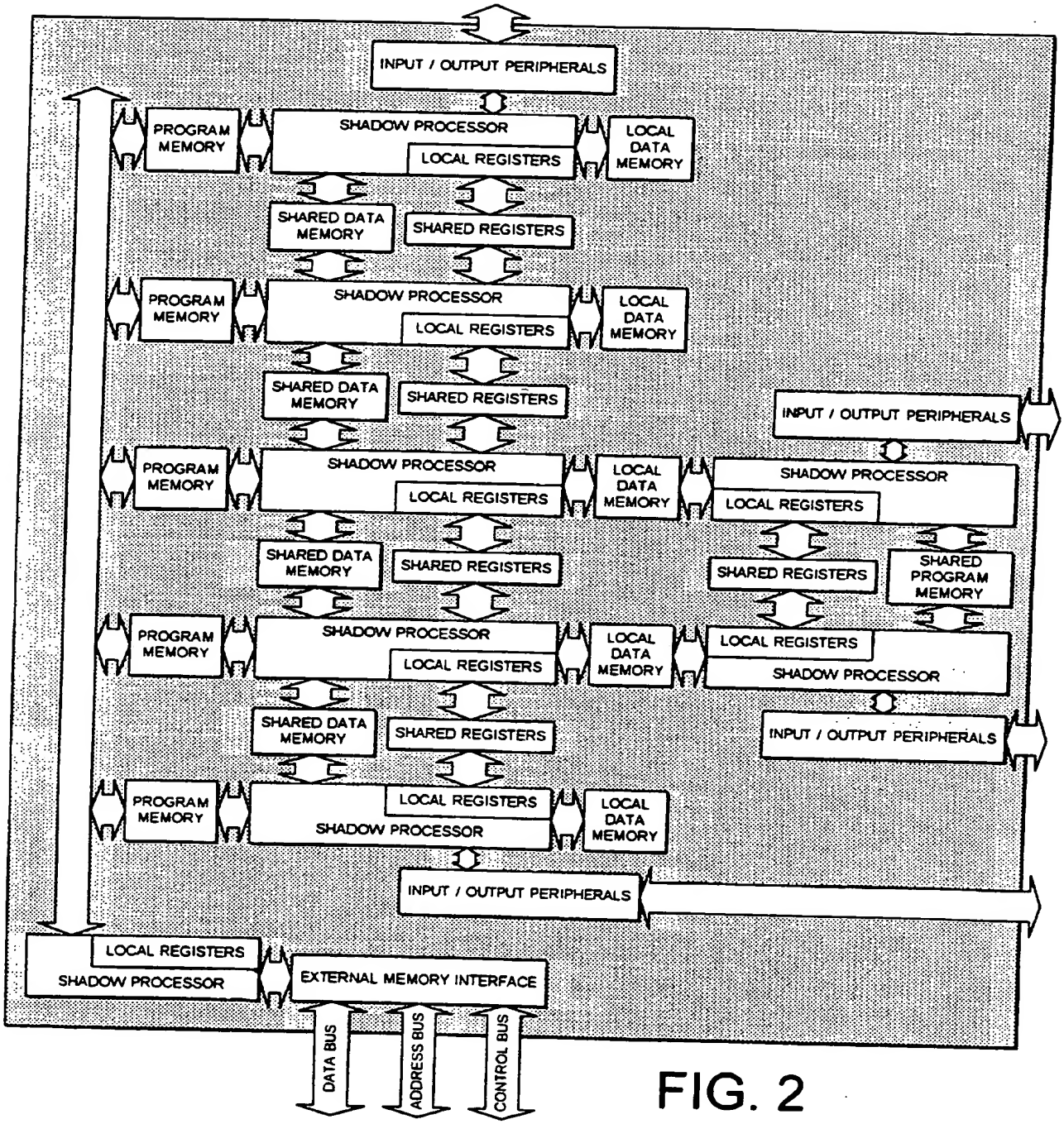

FIG. 2

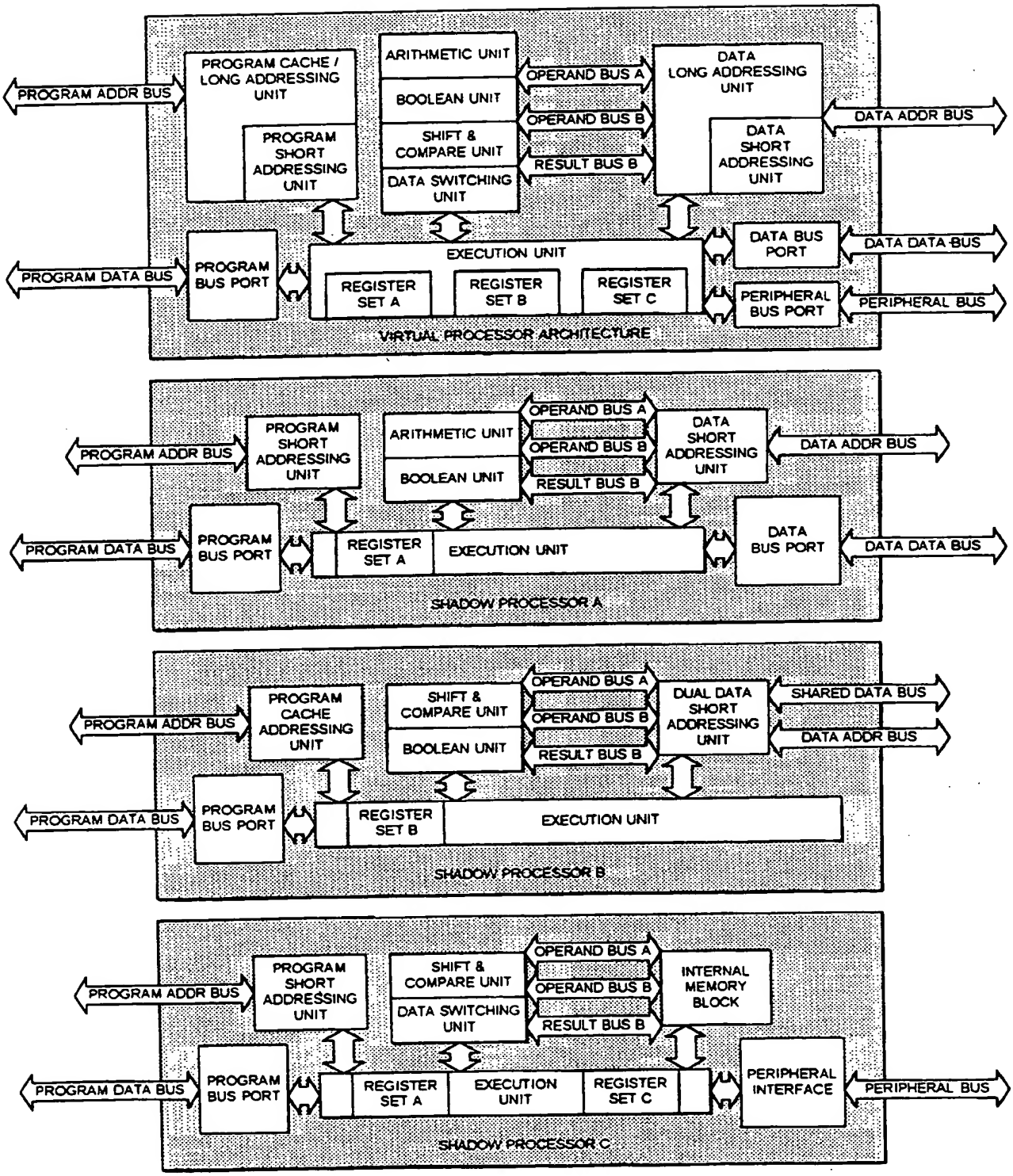
PROGRAM ADDR BUS
PROGRAM CACHE / LONG ADDRESSING UNIT
PROGRAM SHORT ADDRESSING UNIT
ARITHMETIC UNIT
BOOLEAN UNIT
SHIFT & COMPARE UNIT
DATA SWITCHING UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DATA LONG ADDRESSING UNIT
DATA SHORT ADDRESSING UNIT
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
EXECUTION UNIT
REGISTER SET A
REGISTER SET B
REGISTER SET C
DATA BUS PORT
DATA DATA BUS
PERIPHERAL BUS PORT
PERIPHERAL BUS
VIRTUAL PROCESSOR ARCHITECTURE
PROGRAM ADDR BUS
PROGRAM SHORT ADDRESSING UNIT
ARITHMETIC UNIT
BOOLEAN UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DATA SHORT ADDRESSING UNIT
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET A
EXECUTION UNIT
DATA BUS PORT
DATA DATA BUS
SHADOW PROCESSOR A
PROGRAM ADDR BUS
PROGRAM CACHE ADDRESSING UNIT
SHIFT & COMPARE UNIT
BOOLEAN UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DUAL DATA SHORT ADDRESSING UNIT
SHARED DATA BUS
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET B
EXECUTION UNIT
SHADOW PROCESSOR B
PROGRAM ADDR BUS
PROGRAM SHORT ADDRESSING UNIT
SHIFT & COMPARE UNIT
DATA SWITCHING UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
INTERNAL MEMORY BLOCK
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET A
EXECUTION UNIT
REGISTER SET C
PERIPHERAL INTERFACE
PERIPHERAL BUS
SHADOW PROCESSOR C

FIG. 3

PROCESSING ARRANGEMENTS

The present invention relates to processing arrangements for computer architectures.

DESCRIPTION OF THE RELATED ART

There are many conventional computer architectures which are based on a single main processor cooperating with a co-processor. The co-processor adds functionality that the main processor in the architecture does not have or does not perform particularly efficiently. The co-processor generally uses instructions which are not implemented in the instruction set of the main processor. As such, many co-processors are used to address very specific code requirements, for example floating point arithmetic or signal processing. In most applications, this means that the instruction set of the co-processor is specific to that co-processor.

In addition, many main processors use real time operating systems to service multiple tasks and exceptions, such as interrupts. Servicing multiple tasks can result in context changes which can absorb significant amounts of the processing power available in the processor. A context change occurs when the task being executed by a processor is changed. The context of a task relates to the code corresponding to the task, and the state of the internal registers of the processor. Furthermore, in low power applications, in order to conserve power, sleep modes are used from which the processor must be reactivated when interrupt or service requests occur. When the processor is reactivated the context must be loaded and then the service performed, the processor then returns to an inactive state. Such a process can consume a large amount of power.

It is therefore desirable to provide a computer

architecture which can overcome these disadvantages.

SUMMARY OF THE PRESENT INVENTION

According to one aspect of the present invention there is provided a processing arrangement for a computer comprising:

first processor means for processing a first set of instructions; and

second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating a computer processor architecture in accordance with the present invention;

Figure 2 shows a computer architecture including multiple processors; and

Figure 3 is a diagramatic illustration of how processors embodying the present invention can realise the functionality of a desired virtual processor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a block diagram illustrating a host (or first) processor 1 connected with a shadow (or second) processor 2. In the example shown, the shadow processor 2 is used to control interrupts received from peripherals connected to the processor system.

The host processor 1 communicates with an external bus 3 by way of an external bus interface 4. The external bus 3 is used for transferring data to and from the main processor and memory devices (not shown).

The host processor 1 also includes a memory controller 5 for controlling data access with memory devices. The memory controller 5 is controlled itself by an execution unit 6 which has overall control of the main processor 1. The host processor 1 also include an arithmetic logic unit (ALU) 7 and a number of registers 8, sixteen in the example shown. The various components of the host processor 1 communicate with each other by way of appropriate internal buses.

In order that the host processor 1 can be held in a low power inactive mode for as long as possible, a shadow processor 2 is connected to the main processor 1. The shadow processor 2 includes an interrupt controller 10 which receives interrupt signals via interrupt inputs 12. The shadow processor also includes registers which correspond to selected ones of the registers of the host processor 1. The interrupt controller can be connected, as in the example of Figure 1, to peripherals connected to a peripheral bus 11.

The shadow processor 2 also includes an execution unit 14, code memory 15, and data memory 16. The shadow processor 2 operates to process a selected subset of the instructions from which the host processor operates, and these instructions are stored in the code memory 15. The shadow processor 2 has access to the host processor memory by way of a memory controller 17 which interfaces with the external bus 3 by way of the host external bus interface 4.

In order to provide a link between the host processor 1 and the shadow processor 2, the execution units of the two processors are connected by way of a host interrupt controller 18, and the registers of the processors are connected by a register bridge unit 19. The Host Interrupt Controller 18 is a module which

allows the shadow processor to issue an interrupt to the host porcessor in order to cause a change in task execution, a context change, appropriate to the requirements of the system. It generates an interrupt to the host using the host interrupt protocol and indicating the source of the interrupt as a vector programmed by the shadow process related to the new task required.

The following description, of the process used to service an interrupt received from a peripheral bus 11 is one example of the operation of the shadow processor 2. A peripheral (not shown) raises an interrupt request on the interrupt input lines 12. The input controller 10 operates to interpret the interrupt request, and if the interrupt request is of the type able to be processed by the shadow processor 2, then the shadow processor 2 will service that interrupt. An example of an interrupt is if an external device such as a serial port has received data from a system to which it is attached. The data from such a serial port may be contained within a message body including information about the source and content of the data. The shadow processor 2 then services the interrupts required by receiving the message then removing the data from that message. Once the data has been removed and checked it issues an interrupt to the main processor 1 via the Host Interrupt Contoller 18 having first set up the context needed by the task to service the data within the message. The main processor 1 would begin processing the data while the shadow processor 2 stores the context of the interrupted task.

The Register Bridge unit 19 allows multiple access to a set of registers by both host and shadow processor. It allows physical registers to appear in both processor systems while resolving any conflict in

The Patent Office

INVESTOR IN PEOPLE

Application No:	GB 9823819.9	**Examiner:**	David Keston
Claims searched:	1-6	**Date of search:**	22 April 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): G4A (AFGDT, AFGL, AMP)

Int Cl (Ed.6): G06F 9/38, 15/16

Other: Online: COMPUTER, EDOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0174231 A1	(LA TELEMECANIQUE ELECTRIQUE) - see abstract	1, 5
A	US 5588118	(ZILOG) - see abstract	1, 5
A	US 4395758	(DIGITAL EQUIPMENT CORP.) - see abstract	1, 5
A	Computer Shopper, Vol.13, No.1, Jan. 1993, John Bryan, "Low power technology: the 3 volt revolution", p801(4)		3, 4, 6
X	Computer Shopper, Vol.12, No.1, Jan. 1992, Winn L. Rosch, "486: into the mainstream" p487 (11)		1, 5

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

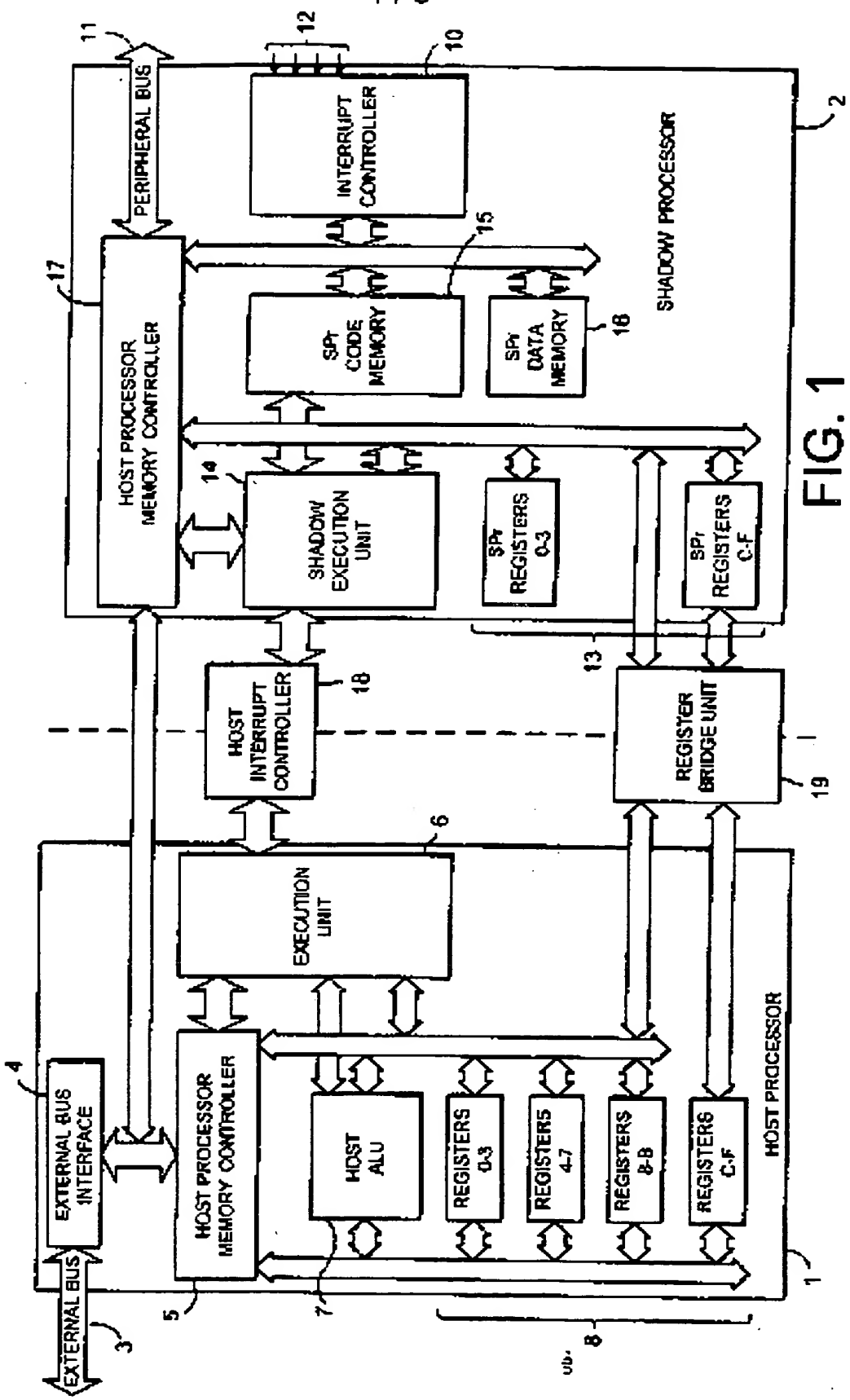

FIG. 1

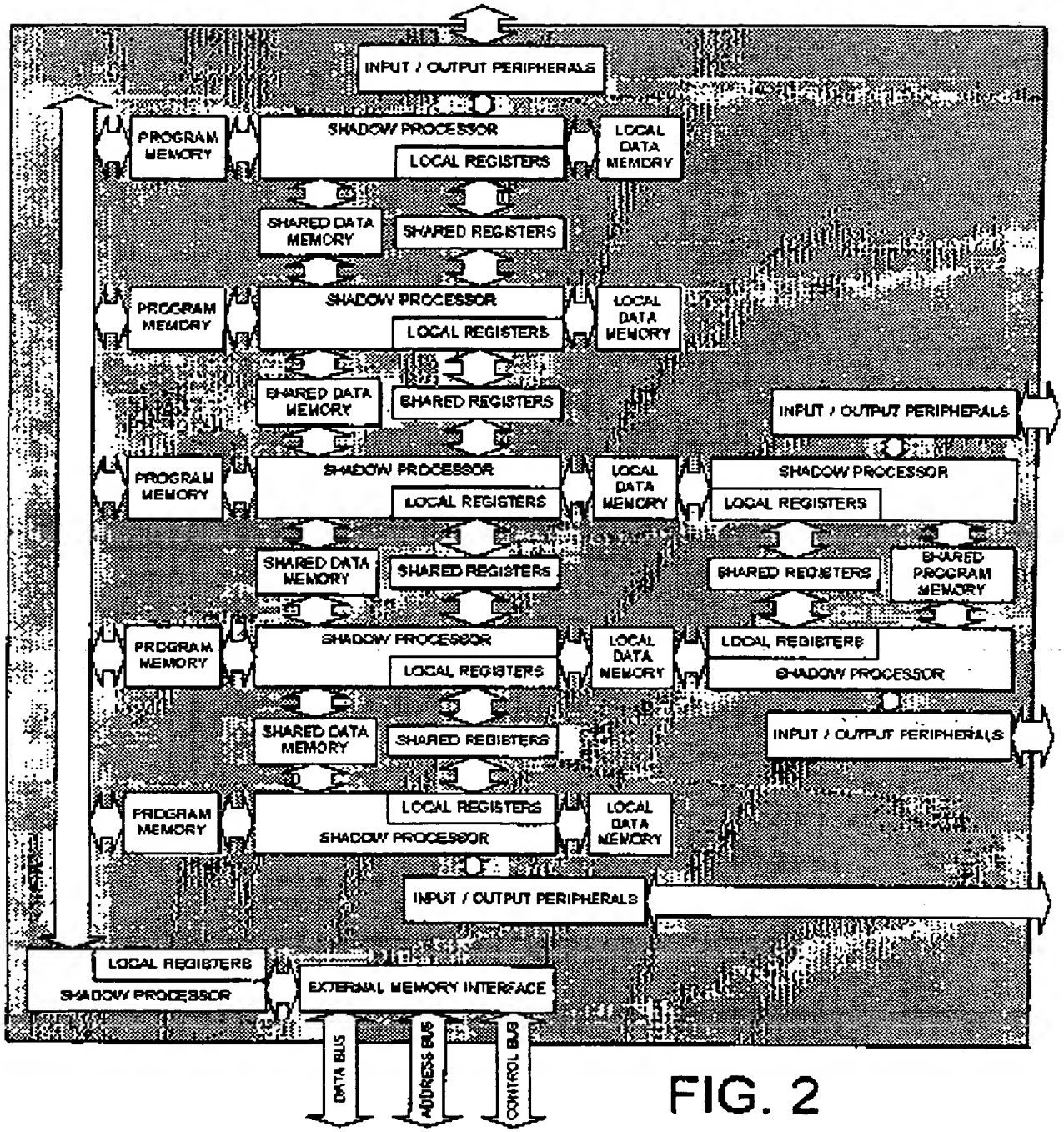

FIG. 2

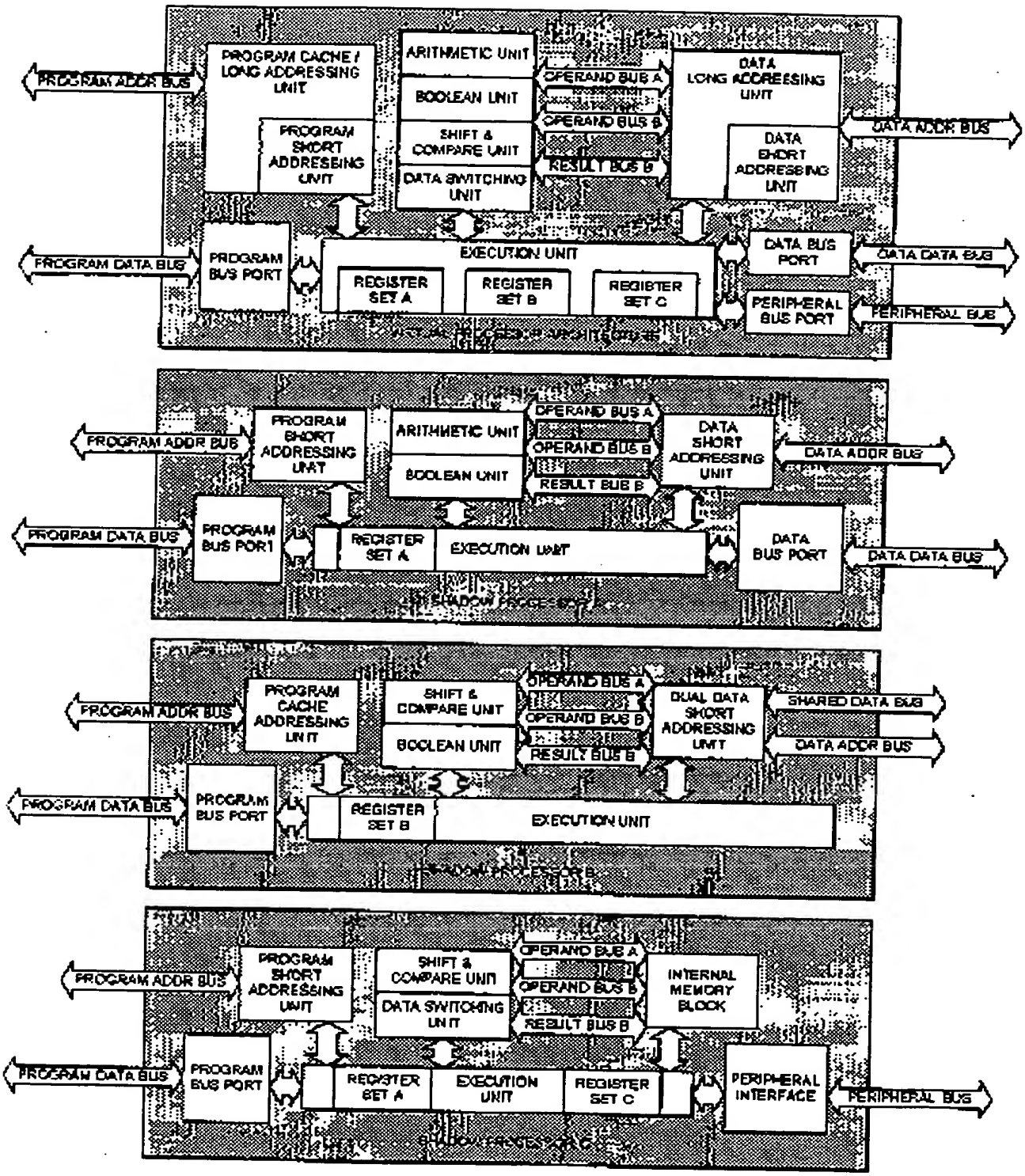

FIG. 3